Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) ~~An apparatus~~A semiconductor chip, comprising:

a capacitive structure, comprising:

a) an inner node, comprising:

a first pair of vertically aligned strips electrically connected with one or more vias, a second pair of vertically aligned strips electrically connected with one or more vias, the higher strips of both of said pairs at a same metal level, the lower strips of both of said pairs at a same lower metal level; ~~and,~~

b) an outer node, comprising:

at said metal level:

a first metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said higher strips, a second of said windows surrounding and isolated from a second of said higher strips;

at said lower metal level:

a second metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said lower strips, a second of said windows surrounding and isolated from a second of said lower strips;

said first and second metal structures electrically connected with one or more vias;

c) a third metal structure at another metal level other than said metal level and other than said lower metal level, said third metal structure at least partially vertically aligned with at least one of said pairs of vertically aligned strips, said third metal structure electrically connected to said inner node; and,

d) a fourth metal structure at said another metal level, said fourth metal structure substantially surrounding said third metal structure on three sides of said third metal structure within the plane of said another metal level to shield said third metal structure, said fourth metal structure electrically connected to said outer node, said fourth metal structure not completely surrounding said third metal structure within the plane of said another metal level.

2. (presently amended) The ~~apparatus~~ semiconductor chip of claim 1 wherein said lower metal level is a second metal level of said semiconductor device and said higher metal level is a third metal level of said semiconductor device.

3. (presently amended) The ~~apparatus~~ semiconductor chip of claim 1 further comprising a first plane of metal that is at least partially vertically aligned with and above said higher strips and said first metal structure.

4. (presently amended) The ~~apparatus~~ semiconductor chip of claim 3 wherein said first plane of metal comprises shielding strips and is electrically connected to said outer node.

5. (presently amended) The ~~apparatus~~ semiconductor chip of claim 1 ~~4 further comprising a second plane of metal that is vertically aligned with and~~ wherein said another metal level is beneath said lower strips and said second metal structure~~, said second plane of metal being electrically connected to said outer node~~.

6. (presently amended) The ~~apparatus~~ semiconductor chip of claim ~~5~~ 1 wherein said ~~second plane of~~ fourth metal structure comprises shielding strips.

7. – 9. canceled.

10. (Original) The apparatus of claim 1 wherein said capacitive structure is part of an Analog-to-Digital Converter (ADC) circuit.

11. (presently amended) A~~n apparatus~~semiconductor chip, comprising:

a capacitive structure comprising, at a same metal level, an outer metal ~~feature~~ structure that forms a window that ~~completely~~ surrounds and is isolated from an inner, ~~rectangular~~ metal strip within the plane of said metal level ~~that runs along a width of said capacitive structure~~, said capacitive structure also comprising, at another metal level, another metal structure that substantially surrounds but does not completely surround an inner metal structure, said another metal structure electrically coupled to said outer metal structure with one or more vias, said inner metal structure electrically coupled to said inner metal strip with one or more vias.

12. (presently amended) The ~~apparatus~~ semiconductor chip of claim 11 wherein said outer metal feature further comprises a second window that ~~completely~~ surrounds and is isolated from a second, inner~~, rectangular~~ metal strip ~~that runs along a width of said capacitive structure~~.

13. (presently amended) The ~~apparatus~~ semiconductor chip of claim 11 further comprising, at a second another metal level and in a location that is vertically aligned with said outer metal ~~feature~~structure, a second outer metal ~~feature~~ structure that is connected to said outer metal ~~feature~~ structure with one or more vias.

14. (presently amended) The ~~apparatus~~ semiconductor chip of claim 12 further comprising, at said second another metal level and in a location that is vertically aligned with said ~~rectangular~~ metal strip, ~~a third metal feature~~ another metal strip that is connected to said ~~rectangular~~ metal ~~feature~~ strip with one or more vias and is isolated from said second outer metal ~~feature~~structure, said another metal strip within a window formed by said second outer metal structure.

15. – 17. (canceled).

18. (Original) The apparatus of claim 11 wherein said capacitive structure is part of an ADC circuit.

19. (presently amended) A machine readable medium having stored thereon instructions which when executed by a computing system cause said computing system to perform a method, said method comprising:

designing a capacitive structure into a design for an electronic circuit, said capacitive structure comprising:

a) a first node, comprising:

a first pair of vertically aligned strips electrically connected with one or more vias, a second pair of vertically aligned strips electrically connected with one or more vias, the higher strips of both of said pairs at a same metal level, the lower strips of both of said pairs at a same lower metal level; ~~and,~~

b) a second node, comprising:

at said metal level:

a first metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said higher strips, a second of said windows surrounding and isolated from a second of said higher strips;

at said lower metal level:

a second metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said lower strips, a second of said windows surrounding and isolated from a second of said lower strips;

said first and second metal structures electrically connected with one or more vias;

c) a third metal structure at another metal level other than said metal level and other than said lower metal level, said third metal structure at least partially vertically aligned with at least one of said pairs of vertically aligned strips, said third metal structure electrically connected to said inner node; and,

d) a fourth metal structure at said another metal level, said fourth metal structure substantially surrounding said third metal structure on three sides of said third metal structure within the plane of said another metal level to shield said third metal structure, said fourth metal structure electrically connected to said outer node, said fourth metal structure not completely surrounding said third metal structure within the plane of said another metal level.

20. (new) The machine readable medium of claim 19 wherein said designing further comprises calculating a width for said capacitive structure.

21. (new) The machine readable medium of claim 19 wherein said designing further comprises calculating a length for said capacitive structure.

22. (new) The machine readable medium of claim 19 wherein said designing further comprises calculating a number of strips of which said vertically aligned strips are included.

23. (new) The machine readable medium of claim 19 wherein said designing further comprises using an equation that includes the capacitance of said capacitive structure.

24. (new) The machine readable medium of claim 19 wherein said designing further comprises using an equation that includes the spacing between metal lines.

25. (new) The machine readable medium of claim 19 wherein said designing further comprises using an equation that includes the width of a metal line.

26. (new) A machine readable medium having stored thereon instructions which when executed by a computing system cause said computing system to perform a method, said method comprising:

designing a capacitive structure into a design for an electronic circuit, said designing comprising:

designing at a same metal level, an outer metal structure that forms a window that surrounds and is isolated from an inner, metal strip within the plane of said metal level;

designing at another metal level, another metal structure that substantially surrounds but does not completely surround an inner metal structure; and,

designing said another metal structure to be electrically coupled to said outer metal structure with one or more vias, and designing said inner metal structure to be electrically coupled to said inner metal strip with one or more vias.

27. (new) The machine readable medium of claim 26 wherein said designing further comprises calculating a width for said capacitive structure.

28. (new) The machine readable medium of claim 26 wherein said designing further comprises calculating a length for said capacitive structure.

29. (new) The machine readable medium of claim 26 wherein said designing further comprises calculating a number of strips of which said vertically aligned strips are included.

30. (new) The machine readable medium of claim 26 wherein said designing further comprises using an equation that includes the capacitance of said capacitive structure.

31. (new) The machine readable medium of claim 26 wherein said designing further comprises using an equation that includes the spacing between metal lines.

32. (new) The machine readable medium of claim 26 wherein said designing further comprises using an equation that includes the width of a metal line.